REMARKS/ARGUMENTS

Claims 88-90-95, and 97-121, 123, and 124 are pending in the application. Claims 88, 90-95, and 97-121 and 123 stand rejected, while claim 124 is objected to as containing allowable subject matter. In response, the subject matter of claims 90 and 124 have been incorporated into claim 88, and claims 90 and 91 have been cancelled. Thus, claims 88, 92-95, and 97-121, 123 and 124 remain pending in the application, with claim 88 being the sole independent claim. Applicants reserve the right to pursue the original claims and alter the claims in this application and in other applications.

Because the Examiner indicated that claim 124 contains allowable subject matter (Office Action mailed September 19, 2002, Paper No. 14, page 13, section 6), claim 124 has been incorporated into claim 88. All claims depend either directly or indirectly from claim 88. Thus, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: December 19, 2002

Respectfully submitted,

By_____

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Version With Markings to Show Changes Made

IN THE CLAIMS:

Please amend claim 88 as follows. Please cancel claims 90 and 91.

88 (amended) A process for forming an interposer element for use as a chip carrier comprising the steps of:

providing an insulating layer on at least one surface of a silicon substrate; and

processing said insulating layer to produce at least one passive circuit element on or within said insulating layer, said at least one passive circuit element being separated from said silicon substrate by a portion of said insulating layer, said portion of said insulating layer having a thickness such that said at least one passive circuit element is electrically shielded from said silicon substrate,

solder bonding at least one integrated circuit chip to said interposer element, by forming a plurality of individual solder ball leads, wherein two or more of said individual solder ball leads use differing types of solder having differing melting points, such that said at least one integrated circuit chip is electrically connected to said at least one passive circuit element; and

forming a metallization pattern on or within said insulating layer, said metallization pattern being connected with said at least one passive circuit element.